HIGH VOLTAGE CMOS PROCESS ACCELERATED OPERATING LIFE TEST RESULT	
Sample Size	3566
Equivalent Device Hours	413 325 827
Failure Rate in FIT	2.202

Failure Rate in FIT is calculated according to JEDEC Standard JESD85, *Methods for Calculating Failure Rates in Units of FITs,* based on accelerated high temperature operating life test results by using an apparent activation energy of 0.7 eV. The junction temperature of the device at use is assumed to be 55 °C. A constant failure rate distribution is assumed. The upper confidence bound of the failure rate is 60 %.